IN THE CLAIMS

1. (Currently Amended) A memory controller, comprising:

an array of tag address storage locations having a count; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module, the memory module coupled to the command sequencer and serializer~~memory controller~~ via a memory bus, each tag address storage location in the array of tag address storage locations corresponding to a cache line, the cache line having a cache line size, the cache line in one of an unsegmented state and a segmented state in which the size of the cache line is one half of the cache line size in the unsegmented state, and further wherein the count of tag address storage locations is invariant between the unsegmented state of the cache line and the segmented state of the cache line.~~divided into two segments.~~

2. Cancelled

3. (Previously Presented) The memory controller of claim 1, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

4. (Previously Presented) The memory controller of claim 3, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

5. (Previously Presented) The memory controller of claim 4, each of the plurality of arrays of tag address storage locations organized into 4 ways.

6. (Currently Amended) A memory module, comprising:

a memory device; and

a data cache coupled to the memory device, the data cache controlled by commands delivered by a memory controller component over a memory bus, the memory controller component including an array of tag address storage locations having a count, each tag address storage location in the array of tag address storage locations corresponding to a cache line having a cache line size, the cache line in one of an unsegmented state and a segmented state in which the size of the cache line is one half of the cache line size in the unsegmented state, and further wherein the count of tag address storage locations is invariant between the segmented state of the cache line and the unsegmented state of the cache line~~divided into two segments~~.

7. Cancelled

8. (Previously Presented) The memory module of claim 6, the data cache organized into a plurality of ways.

9. (Previously Presented) The memory module of claim 8, the data cache organized into 4 ways.

10. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including an array of tag address storage locations having a count; and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

a memory module coupled to the memory controller via a memory bus, the memory module including

a memory device, and

a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, each tag address storage location in the array of tag address storage locations corresponding to a cache line, the cache line having a cache line size, the cache line in one of an unsegmented state and a segmented state in which the size of the cache line is one half of the cache line size in the unsegmented state, and further wherein the count of tag address storage locations is invariant between the unsegmented state of the cache line and the segmented state of the cache line~~divided into two segments~~.

11. Cancelled

12. (Original) The system of claim 10, further comprising:

a plurality of arrays of tag address storage locations, each of the plurality of arrays of tag address storage locations corresponding to one of a plurality of memory modules.

13. (Original) The system of claim 12, each of the plurality of arrays of tag address storage locations organized into a plurality of ways.

14. (Original) The system of claim 13, each of the plurality of arrays of tag address storage locations organized into 4 ways.

15. (Original) The system of claim 14, a point-to-point interconnect to couple the memory controller to the memory module.